2 and 4 Watt Ka-band GaAs PHEMT Power Amplifier MMICs

Francois Y. Colomb and Aryeh Platzker

Raytheon RF Components, Andover, MA 01810, USA

Abstract — **The design and performance of power amplifiers for Ka-band applications is presented. A three-stage amplifier demonstrated 22 dB small signal gain from 26.5 GHz to 31.5 GHz and saturated output power of 4W with 28% power added efficiency from 28 GHz to 31 GHz. Record power density of 670 mW per mm of device output periphery was achieved. The amplifiers were fabricated on a selective double-recess 0.2 μm GaAs power pHEMT process.**

I. Introduction

Power amplifiers are needed for new generations of commercial and military Ka-band communications systems requiring high linearity. Advances in semiconductor devices and fabrication processes have enabled viable solid-state implementations of power amplifiers. Powers at the MMIC level are in the order of one to several Watts. Table I gives an overview of some of the best results reported to date [1-7].

The amplifiers presented in this paper were designed for operation under variable drain voltages over wide frequency range with acceptable linearity. These features offer several system advantages such as higher efficiency and economy of implementation. The performance of our circuits advances the state of the art of Ka-band amplifiers.

II. PHEMT Process

The MMIC amplifiers were fabricated on Raytheon's selective double-recess, 0.2μm T-gate power GaAs pHEMT process with 25μm individual source vias [8]. The first recess dimension is ~0.8 μm. The device layout includes 2.2μm S-D and 30μm G-G spacings. Gold metalizations include 1μm cap bottom and 3μm thick top layers. The wafers are thinned to 50 μm prior to via etch and backside metalization. The process includes 6Ω/sqr Tantalum Oxide resistors and 0.2μm SiN passivation providing 0.3fF/μm^2 MIM capacitors.

Fig. 1 shows DC and pulsed IV characteristics of a typical 6x100μm device. Typical device parameters are:

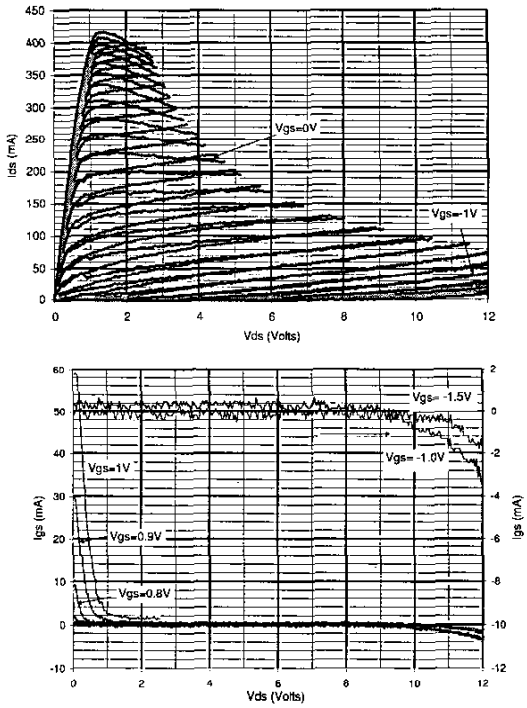

Fig. 1 DC and pulsed IV characteristics. −1.5≤Vgs≤ 1V, 0.1V steps. Pulse bias: 5Vds, -0.431Vgs, 109mA, 1μs wide; a) Drain current vs drain voltage, b) Gate current vs drain voltage.

TABLE I. Comparison of Ka-band Power Amplifier MMICs

Psat Power		P1dB Power		Power per	Min.	Power	Drain	Sm. Sig.	Sm. Sig.	No.	Output	Power/Out-	Chip	Process		Corp.	Date ·
Watt	dBm	Watt	dBm	Out. Periph. mW/mm	PAE %	Bandw. GHz	Volt. V	Gain dB	Band GHz	Sta-ges	Periph. mm	put Periph. mW/mm	Area mm^2	Substr - mil	Gate μm		Reference
4.0 - 4.3	36.0-36.3	3.2-3.5	35.0-35.5	620-670	28	28-31	6	23	26.5-32.5	3	6.4	620-670	16.2	2	0.2	RTN	This work
1)	1)	2.3-3.2	33.6-35.0	200-275 2)	1)	27-31	6	23	24-31	4	11.52	200-275 2)	13.0	2	0.25	TQNT	2002 [1]
1)	1)	2.8	34.5	245 2)	23	28-30.5	6	18	28-31	3	11.52	245 2)	13.0	2	0.25	TQNT	2002 [2]
.72 - .91	28.6-29.6	0.6-0.8	28.0-29.0	300-380	17	28-31.5	6	16	26-36	4	2.4	300-380	2.3	2.75	0.25	UMS	2002 [3]
5.9	37.7	1)	1)	400	21	30-31	7	21.5	25-31	3	14.72	400	26.3	1)		MOT	2001 [4]
2.8-4.5	34.5-36.5	2.2-3.5	33.5-35.5	350-560	25	29-32	5	15	1)	2	8.0	350-560	14.9	2	0.15	LMT	1999 [5]
1.6-2.0	32.0-33.0	0.9-1.3	29.5-31.0	410-520	24	29.5-31.5	5.5	19		2	3.84	410-520	12.1	4	0.15	TRW	1999 [6]
1)	1)	1.4	31.6	600 2)	24	@ 30 GHz	6	10	27-31	2	2.4	600 2)	3.9	4	0.2	MIEL	1998 [7]

1) Not Reported 2) P1dB power density

0-7803-7695-1/03/$17.00 © 2003 IEEE

DC, pulsed Imax ~690, 630 mA/mm; V_{gsBD}~10-11V; max. g_m @6Vds~500mS; Vpo~-0.9V. Reliability studies of amplifiers indicate RF power degradation rates of ~0.5dB/10^5 hours at Vds=5 and 6V.

III. Circuit Design

Four three-stage amplifiers sharing the same general topology were designed for approximately 2 and 4W output power levels. The higher power level was achieved by increasing the unit gate width of the pHEMTs from 60 µm to 100 µm and modifying the matching networks for the new impedances. A chip photo is shown in Fig. 2, amplifiers partition in Table II.

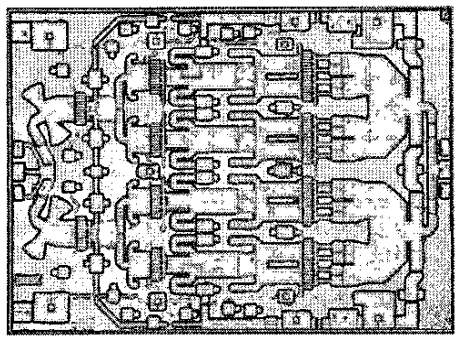

Fig. 2. 4W Amplifier MMIC. Size: 4.8mm x 3.4mm.

TABLE II. Amplifier Partition

Power Level	1st Stage	2nd Stage	3rd Stage	3rd Stage Periphery	Total Periphery
2 Watt	2(10x60µm)	4(10x60µm)	4(16x60µm)	3.84 mm	7.44 mm
4 Watt	2(10x100µm)	4(10x100µm)	4(16x100µm)	6.4 mm	12.4 mm

A. Output Combiner Design

For each power level, two values of load resistance of the output devices, 13 and 17Ωmm were used to cover operation over variable Vds. The target parallel load capacitance was –0.33 pF/mm for all amplifier stages. This value essentially cancels the device's output capacitance, estimated as C_{ds} + C_{dg} and confirmed with load pull measurements.

For the design of the output matching network, each 16-finger device was considered as two devices of 8 fingers each. The output was thus modeled as an 8-to-1 combiner. The ability to control the impedance at the output of each device in the presence of all the others is critical. Differences in impedance cause asymmetry of the output stage leading to early compression and reduced overall performance. In the fully connected amplifier, these impedances depend in general on the devices excitations, their source impedances, and the properties of the combiner. This situation is similar to the embedded input impedances of a small array of antennas with mutual coupling between elements.

Simulations of load resistance and parallel capacitance for the 4W design and 17 Ωmm target are shown in Fig. 3. Due to the combiner symmetry, there are only four unique embedded impedances.

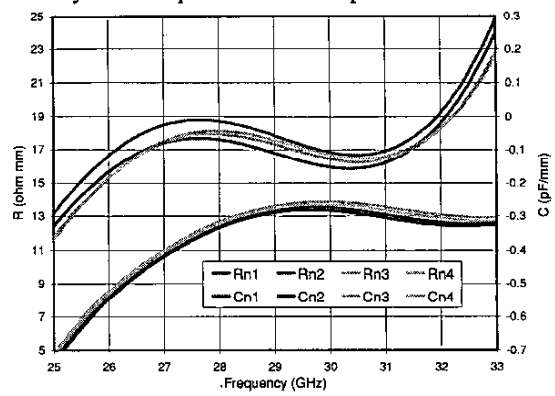

Fig. 3. Simulated load resistance and load capacitance for 4W design with 17 Ωmm load resistance target.

B. Interstages and Input Matching Network Design

Gain, power and efficiency must be considered simultaneously during the design of the interstages. The load impedance and periphery of each stage must be chosen such that enough power is available for driving the subsequent stage. Building in margin to account for processing variation and modeling uncertainty is key to success.

The input matching network is designed last and functions to ensure proper input match and overall gain response. Both input and output matching networks take into account a short wire-bond connection of 175pH (j33Ω) to a 50Ω load. Failure to include this effect at the onset could spell disaster.

Stability of the amplifier was verified using the normalized determinant function (NDF) method [9,10]. Small resistors are placed in series with the DC gate bias lines connecting each device and between the drains of the devices to prevent odd mode instabilities.

C. EM Simulation

It is clear by inspecting Fig. 2 that a design approach based solely on piecing together a circuit with predetermined library models would not be adequate at these frequencies.

We enhanced the accuracy of the schematic description with EM simulation and a simple mapping technique. Most of the design and optimization was

then performed with the standard optimization features of the linear circuit simulator.

EM simulation with Agilent ADS Momentum and Sonnet *em* was used for all RF parts of the networks. Both tools were used to take advantage of strengths and avoid limitations. We believe that the extensive EM simulation used contributed greatly to the first-pass design performance presented in this paper.

D. Special Passive Components

A distinct characteristic of the present designs is the use of interdigitated capacitors to produce accurate and repeatable capacitances for matching elements in the interstage and input networks. This was done to eliminate the sensitivity associated with the small MIM capacitors that would be needed in these places. EM simulation of the interdigitated capacitors is necessary since the accuracy of the library models is inadequate.

Large RF bypass capacitors in the output drain bias lines were tucked under the lines to save area. The distributed effect can be predicted with a simple multiple transmission-line model or with EM simulation.

Wide transmission line transformers are used in many places and contribute to the wide frequency bandwidth of the amplifier.

IV. MEASUREMENTS

The MMICs were soldered onto 90W/10Cu carriers and evaluated in 2.4mm test fixtures. 100pF and a 10μF bypassing capacitors were added to the gate and drain connections and are mounted directly on the carrier in close proximity to the MMIC. All the measurements presented below are referenced to the coaxial ports thereby including all fixture losses.

A. Small Signal Performance

Typical S-parameters of the 17Ωmm 4W design are shown in Fig. 4 for drain bias of 6V and quiescent current of 1.8A.

All amplifiers have BPF responses with no undesired out-of-band peaks. Over 26.0 - 32.5 GHz, the 4W MMICs exhibit 21 to 26dB of gain and max. in-band input and output return losses of 5 and 9 dB. Over 27.5 - 33 GHz, the 2W MMICs exhibit 23 to 31dB of gain and max. input and output return losses of 4 and 3 dB.

B. Power Performance

Output powers and efficiencies were measured over 2-6Vds and 95-160mA/mm Idsq. Typical saturated performances of 2 and 4W high load resistance MMICs are shown in Fig. 5. The data compares favorably with

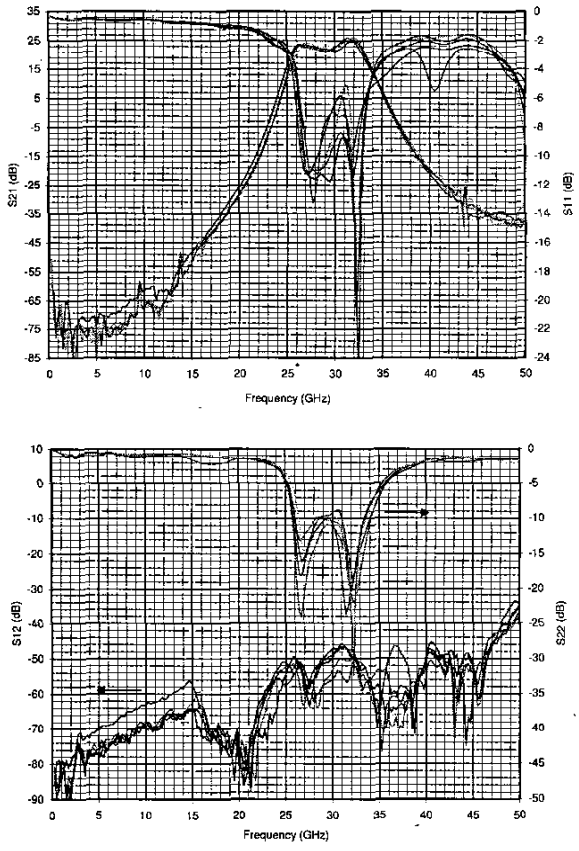

Fig. 4. Magnitude of S-parameters of 5 fixtured MMICs with 17Ωmm load resistance; Vds=6V, Ids=1800mA.

the expected variation of 20log(V1/V2) of a fixed load device. At Vds=6V, the 2W amplifier Psat is 2W min. with 18% min. PAE from 27.2 - 33.4GHz. In the narrower frequency interval of 28.3 - 30.9 GHz, Psat is 2.5W (34 dBm) with 22% PAE min.. The PAE reaches an overall maximum of 32% at 30 GHz for Vds=5V.

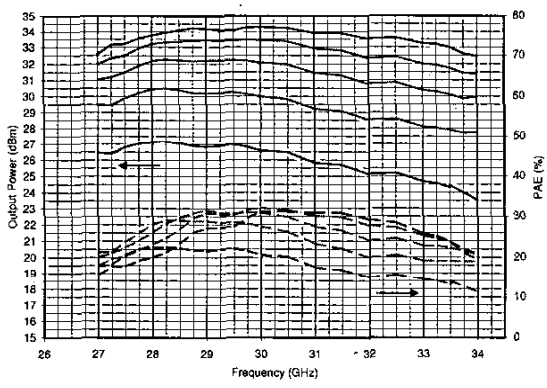

Fig. 5a.

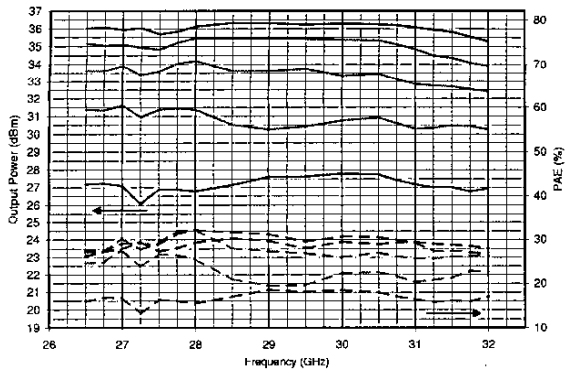

Fig. 5. Saturated powers and efficiencies of 17Ωmm load resistance circuits at Vds=2,3,4,5,6V. (a) 2W MMIC, Idsq= 1.4A; Vgs=-0.51V. (b) 4W MMIC, Idsq=1.8A; Vgs=-0.48V.

The 4W amplifier Psat is 4W min. with 28% PAE from 28 - 31 GHz. The overall maximum PAE is 32% at 28 GHz for Vds=5V. The overall maximum power is 36.3 dBm (4.3 Watt) resulting in a power density of 680mW/mm of output periphery. To the authors knowledge this is the highest power density/efficiency combination reported for a MMIC at this frequency.

C. Two-Tone Excitation

The amplifiers were subjected to two-tone excitations over the same range of Vds and Idsq as power. With proper external bypassing, the 3rd-order intermods were substantially the same over 10kHz to 100MHz tone separations. Typical 3rd-order intermod performances of the 4W 17Ωmm design are shown in Fig. 6.

ACKNOWLEDGEMENT

The authors wish to acknowledge the support of R. T. Keenan from Raytheon Network Centric Systems and the assistance of Dr. K. Alavi, C.D. Alfaro, C.C. Tilas, S.M. Camasso, D.A. Loo, C.Y. Son, T.M. Charbonneau.

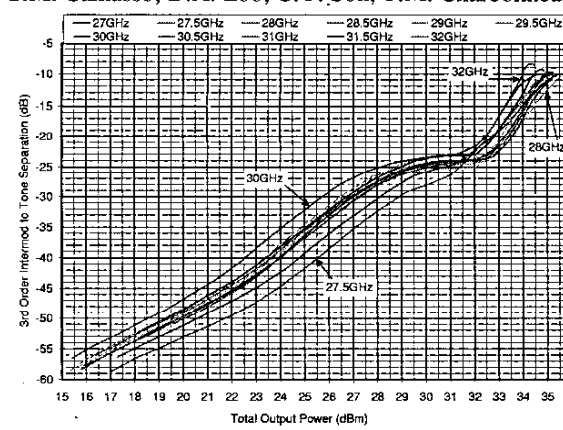

Fig. 6a.

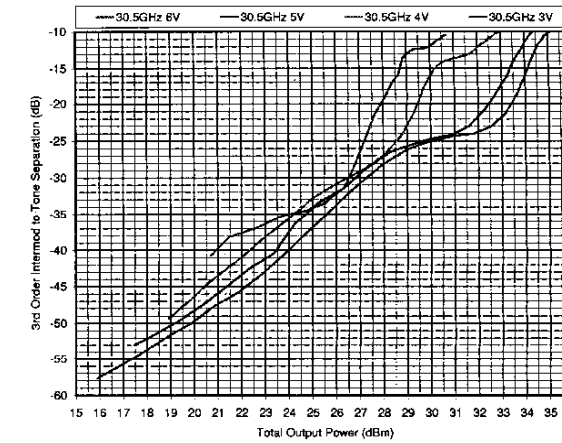

Fig. 6b.

Fig. 6. 3rd Order intermodulation products from 2-tone excitations (Δf=10MHz) of 4W 17Ωmm MMIC as a function of total output powers. (a) Over 28-32 GHz at Vds=6V, Idsq=1.6A. (b) At 30.5 GHz, Vds=3,4,5,6V, Idsq=1.6A.

REFERENCES

[1] K.-S. Kong, D. Boone, M. King, B. Nguyen, M. Vernon, E. Reese, and G. Brehm, "A compact 30 GHz MMIC high power amplifier (3W CW) in chip and packaged form," *2002 GaAs IC Symp. Dig.*, pp. 37-39

[2] Triquint TGA4501-EPU Data Sheet.

[3] A. Bessemoulin, J. Dishong, G. Clark, D. White, P. Quentin, H. Thomas, D. Geiger, "1-Watt broad Ka-band ultra small high power amplifier MMICs using 0.25-μm GaAs PHEMTs," *2002 GaAs IC Symp. Dig.*, pp. 40-43.

[4] R. Emrick, "Monolithic 6W Ka-band high power amplifier," *2001 IEEE MTT-S. Dig.*, pp. 527-529.

[5] J. J. Komiak, W. Kong, P. C. Chao, and K. Nichols, "Fully monolithic 4 Watt high efficiency Ka-band power amplifier, "*1999 IEEE MTT-S. Dig.*, pp. 947-950.

[6] M. K. Siddiqui, A. K. Sharma, L. G. Callejo, R. Lai, "A high power broadband monolithic power amplifier for Ka-band ground terminals," *1999 IEEE MTT-S Dig.*, pp. 951-954.

[7] M. Komaru, H. Hoshi, H. Kurusu, Y. Notani, T. Katoh, T. Ishida, T. Oku, T. Ishikawa, Y. Mitsui, "1-Watt compact Ka-band MMIC power amplifiers using lumped element matching circuits," *1998 IEEE MTT-S Dig., pp. 1659-1662.*

[8] K. Alavi, D. Shaw, A. Platzker, B. Rizzi, S. Ogut, and R. Puente, "A very high performance, high yield, and high throughput millimeter wave power pHEMT process technology," *2001 GaAs Mantech Dig.*, pp. 105-107.

[9] A. Platzker, W. Struble, and K. T. Hetzler, "Instabilities diagnosis and the role of K in microwave circuits," *1993 IEEE MTT-S Dig.*, pp. 1185-1188

[10] W. Struble and A. Platzker, "A rigorous yet simple method for determining stability of linear N-port networks and MMIC application," *1993 GaAs IC Symp. Dig.*, pp. 251-254.